electrolytic solution and the wafer and thereby deposit a plated layer electrolytically on the wafer;

after a predetermined time, increasing the current flow to a second current density greater than the first current density.

REMARKS
(Petition To Declare An Interference
With U.S. Patent No. 6,074,544)

By virtue of the present amendment, claims 54-59 have been added. Claim 54 has been copied verbatim from U.S. Patent No. 6,074,544 ("the '544 patent"), and applicants respectfully request that the Examiner declare an interference between the above-identified application and the '544 patent. In that regard, it will be noted that the present application is a continuation of U.S. Application Serial No. 09/018,783, filed February 4, 1998, a date well before the July 22, 1998 filing date of the '544 patent. Thus, applicants are senior by approximately five months.

In the interest of completeness, applicants hereby advise the Examiner that the '544 Patent has been asserted against the assignee of the present application in a

counterclaim in an action between Semitool, Inc. and Novellus Systems, Inc., now pending in the U.S. District Court for the District of Oregon in Portland. Applicants' assignee, Semitool, has asked the District Court in Portland to stay the action pending a determination of the interference proceeding. Novellus, the owner of the '544 patent, has resisted Semitool's motion to stay on a number of grounds, including the argument that the Patent and Trademark office is incapable of resolving the issue of whether an interference should be declared in less than two years. Semitool therefore respectfully requests the Examiner to give this matter his earliest possible attention.

While more than a year has passed since the issuance of the '544 patent, Semitool, Inc. has had pending claims to the same invention since at least as early as June of 2001. In that regard, the Examiner's attention is invited to the preliminary amendment filed in this application on June 12, 2001, in which claims to the same invention, namely deposition of metal layers on semiconductor wafers using low current initiation techniques are, and have been, presented. As a result, there is no issue under 35 U.S.C. § 135, the statute of repose.

It is of course clear that both the present application, as well as the parent thereof, Application Serial

No. 09/018,783, filed February 4, 1998, support the claims copied from the '544 patent. Support for the copied claims in the present application is set forth in the following table:

Claim 1 of the '544 patent	Specification of the present application
A method of depositing a metal layer on a semiconductor wafer comprising:	The application describes a method for "filling recessed microstructures" of a "semiconductor wafer" (p. 5, lines 2 et seq.), to deposit a metal layer, namely copper, on the semiconductor wafer.
depositing a seed layer on a surface of the wafer;	The application discloses, (p. 5, lines 13 et seq.) providing a "seed layer for subsequent electrochemical copper deposition".
immersing the wafer in an electrolytic solution containing metal ions;	The present application also describes immersing the wafer in the electrolytic solution. The specification teaches (p. 9, lines 14et seq.) contacting the wafer with the electroplating solution. In addition Fig. 1 of the drawing shows the wafer W immersed in the plating liquid (p. 9, lines 14 et seq.), describing the bottom surface of the wafer W in contact with electroplating solution. The present application describes the electrolytic solution as containing metal ions, namely copper ions (p. 15, lines 5 et seq.).
biasing the wafer negatively with respect to the electrolytic solution so as to create a current flow at a first current density between the electrolytic solution and	The present application discloses biasing the wafer negatively relative to the electrolytic solution to create a current flow at a first current density; the density is 3.2 mA/cm^2. The present application describes that first

the wafer and thereby deposit a plated layer electrolytically on the wafer;	stage as a "low plating current" (p. 16, lines 1 et seq.), serving to electrolytically deposit copper on the wafer.
after a predetermined time, increasing the current flow to a second current density greater than the first current density.	The present application describes a "low current initiation" process, which proceeds for a predetermined period of time such as 30 seconds, followed by a "high current plating" process. The specification states that the majority of the copper is plated during that plating process in which the high current density is employed. Thus the specification teaches (p. 16, lines 1 et seq.) the first stage using a low current initiation process whereas the next stage is a high current plating process.

Respecting that last clause, the Court in Portland has reached a tentative claim construction that the phrase "after a combined thickness of the seed and plated layers has reached a predetermined value" means that the "thickness is monitored in some manner so that the current flow is increased only after the combined thickness of the seed and plated layers has reached a predetermined value. A 'value' is a quantitative measurement." Under that construction, claim 1 of the '544 patent is supported by the present specification.

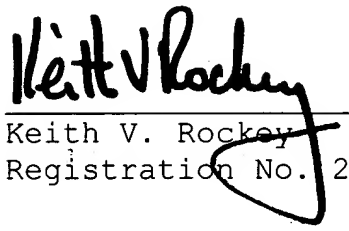
The remaining claims are supported herein for the same reasons as set forth in the proceeding table. Claim 55 is copied verbatim from claim 4 of the '544 patent, specifying that

both the plated metal and the metal constituting the seed layer include copper. Those limitations are supported by the present application as well as its parent at, for example, page 12, lines 7 et seq. of the present application, describing the use of copper for the seed layer. The very next paragraph, lines 14 et seq., describes the step of electrochemical copper deposition as the plating operation. Claim 56 is copied from claim 5 of the '544 patent and is supported by the same disclosure at page 12. The remaining claims are supported in the same way for the same reasons as described above.

The Examiner thus should declare an interference between the present application and the '544 patent. The count should be claim 1 of the '544 patent verbatim and each of the claims 1-7 of the '544 patent should be designated as corresponding to the count. Similarly, all of the claims presented in the present application, claims 54-59 should likewise be designated as corresponding to the count.

Attached hereto is a clean copy of the claims added, namely claims 54-59. That document is labeled as "Added Claims".

Respectfully submitted,



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ADDED CLAIMS

54. (New) A method of depositing a metal layer on a semiconductor wafer comprising:

depositing a seed layer on a surface of the wafer;

immersing the wafer in an electrolytic solution containing metal ions;

biasing the wafer negatively with respect to the electrolytic solution so as to create a current flow at a first current density between the electrolytic solution and the wafer and thereby deposit a plated layer electrolytically on the wafer; and

after a combined thickness of the seed and plated layers has reached a predetermined value, increasing the current flow to a second current density greater than the first current density.

55. (New) The method of claim 32 wherein the plated and seed layers include copper.

56. (New) The method of claim 32 wherein a top surface of the semiconductor wafer includes features to be filled with metal and the method includes applying a current flow at a third current density such that features are filled with metal.

57. (New) The method of depositing a metal layer on a semiconductor wafer comprising:

immersing a wafer having a seed layer on the surface thereof in an electrolytic solution containing metal ions;

biasing the wafer negatively with respect to the electrolytic solution so as to create a current flow at a first current density between the electrolytic solution and the wafer and thereby deposit a plated layer electrolytically on the wafer; and

after a predetermined time, increasing the current flow to a second current density greater than the first current density.

58. (New) The method of depositing a metal layer on a semiconductor wafer comprising:

56. (New) The method of claim 32 wherein a top surface of the semiconductor wafer includes features to be filled with metal and the method includes applying a current flow at a third current density such that features are filled with metal.

57. (New) The method of depositing a metal layer on a semiconductor wafer comprising:

immersing a wafer having a seed layer on the surface thereof in an electrolytic solution containing metal ions;

biasing the wafer negatively with respect to the electrolytic solution so as to create a current flow at a first current density between the electrolytic solution and the wafer and thereby deposit a plated layer electrolytically on the wafer; and

after a predetermined time, increasing the current flow to a second current density greater than the first current density.

58. (New) The method of depositing a metal layer on a semiconductor wafer comprising:

applying a plating current to the wafer so as to create a current flow at a first current density between the electrolytic solution and the wafer and thereby deposit a plated layer electrolytically on the wafer;

after a predetermined time, increasing the current flow to a second current density greater than the first current density.